Using a Digital Channel of a Test System as an Analog Reference for Wireless SOC Testing

Roger McAleenan and Joe Kelly
Agilent Technologies
South Plainfield, NJ
Email: joe_kelly@agilent.com

Abstract

For SOC devices, it is sometimes required to route high frequency analog signals (>10MHz) to the device under test (DUT). It is common to use an analog signal generator within the test system to provide these signals. However, production test systems for such devices often contain many more digital pins than analog signal generators. Therefore, it is advantageous to utilize the digital pins whenever possible in order to leave the analog resources available for other needs. This work reports how a digital channel (pin) of an SOC test system can be used, leaving the analog signal source available for other purposes. This solution may be used to provide something as simple as a clock pulse or a filtered CW tone. One common need for a high frequency analog signal is when supplying the DUT with an analog reference clock signal for the phase-locked looped functionality within the DUT. This low-level sinusoidal-like signal must be extremely stable with low phase noise. One of the most critical items of concern in these applications is the phase noise of the signal. This will be explored in this paper.

Introduction

Traditional radio architectures for wireless communications devices often incorporate the requirement of having a reference signal, or reference clock for phase-locked loop circuitry of the device. It is essential that this reference signal is a high quality well-characterized waveform. In the end application, the signal is usually produced via a crystal oscillator such as a quartz crystal along with its associated circuitry on the chip. Common operating frequencies of reference clocks are in the 15 to 50 MHz range. Traditionally, this has been due to the excellent quartz performance and low cost.

In the case of production testing, in an effort to minimize load board complexity due to extra components, a signal from the test system may be routed to the device under test (DUT) to act as the crystal reference. Furthermore, in many applications it is not necessary that this signal even be an analog signal. Recently, work has shown that a digital signal from a test system digital channel (pin) can act as the reference clock. Often, digital pins can have equivalent or better performance than an analog signal when used in this application (phase-locked loop reference clocks).

Furthermore for production testing, it is necessary that the DUT and the test system hardware be synchronized. If a digital pin is utilized for the DUT reference clock, it follows that the DUT will be automatically synchronized to the time-base of the test system, allowing accurate assessment of any signals processed by the test system digitizers.

The Phase-Locked Loop

The phase-locked loop (PLL) is a frequency synthesis and control circuit found on the SOC device. It allows a large number of frequencies to be synthesized from one circuit. The primary purpose of a PLL is to provide multiple, stable frequencies on a common time-base (that of the reference clock) within the same system to allow frequency synthesis and frequency multiplication and division. Within an SOC device, the PLL generates the local oscillator (LO) frequency to be used with the mixers in either heterodyne or Zero-IF transmitters or receivers. A basic PLL consists of a reference clock, phase detector, loop filter, and a voltage controlled oscillator (VCO) as shown in Figure 1a.

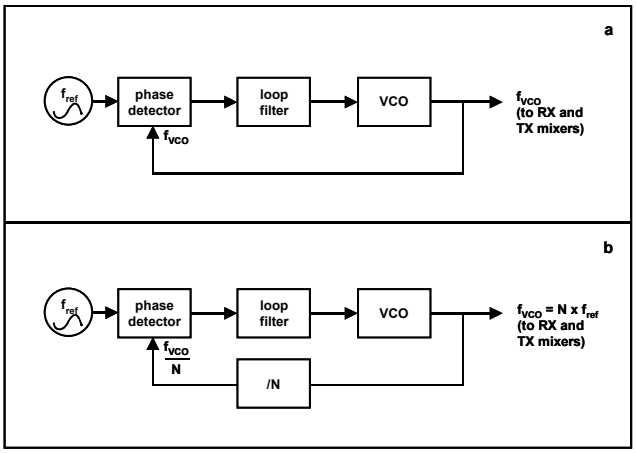

Figure 1 Types of phase-locked loops used in SOC devices; a. basic PLL circuit b. Fractional-N PLL circuit.

Referring to Figure 1a, the principle of operation of a PLL begins with the goal of achieving a stable frequency at the output of the VCO. In this simplest description, the VCO is first set to output a signal with a frequency equal to that of the reference clock. The reference clock is used as a reference for the phase detector, which compares the phase of the reference clock with the negative feedback from the VCO output. If there is a difference in phase between the reference clock and the feedback from the VCO, the output voltage of the phase detector will cause the VCO to deviate toward the reference clock frequency until it "locks" onto it. A filter (termed "loop filter") is used to smooth the pulsed output of the phase detector so that the VCO receives a clean control voltage.

A more common PLL implementation, the Fractional-N PLL is shown in Figure 1b. This permits the use of only one reference clock to produce the numerous frequencies used by the LO during modulation and demodulation of signals in the DUT. In this case, an integer divider is placed into the negative feedback path from the VCO. The divider divides the frequency of the VCO output by N and feeds back the new signal to the phase detector. Assume, for example that the operating frequency of the VCO is N multiples of the reference clock frequency. Then the phase detector input from

the VCO, after dividing by N is once again the frequency of the reference clock. The phase detector then stabilizes the signal to that of the reference clock. Essentially, this method "tricks" the phase detector into believing that the VCO output frequency is at that of the reference clock. The divider is typically digitally controlled and can have any number of values. For wireless communications systems, an upper limit of about 30000 is placed on N due to the introduction of excessive phase noise from frequency multiplication by N [1].

The Importance of Phase Noise

In a PLL the phase noise of the VCO mimics the phase noise characteristics of the reference clock. This is why the phase noise of the reference clock is a critical parameter.

Figure 2 shows the phase noise of a high performance quartz crystal oscillator. The trace shows the excellent stability and close in phase noise that is very low. Such a plot is commonly used to show the overall performance of a signal at different offsets from the carrier. To an RF or mixed signal engineer, the notion of measuring phase noise of a digital signal may seem strange. However, the general concept of phase noise has an analogy in the digital world, i.e., jitter. However, jitter historically has little meaning to an analog signal and furthermore, phase noise information cannot be extracted from jitter measurements [2].

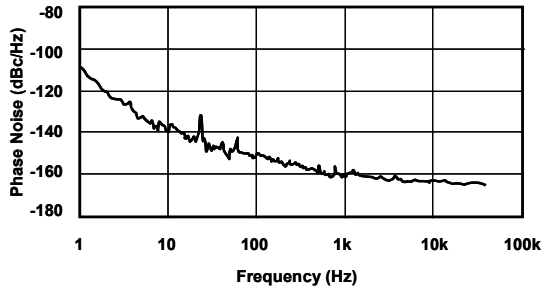

Figure 2 Phase noise plot of a crystal oscillator showing excellent close-in phase noise

Table 1 System specifications for common wireless radio formats

Parameter	DECT	WLAN 802.11a/g	WCDMA
Modulation Format	GFSK	OFDM	OC-QPSK
Bandwidth (MHz)	1.728	16.6	3.84
Noise Figure	18	6.5	9
Sensitivity (dBm)	-83 @BER=10^{-3}	-82 @6Mbps	-110 @BER=10^{-3}
Max input (dBm)	-23	-10	-25
LO Phase Noise (dBc/Hz)	-99 @2.2MHz	-128 @10MHz	-132 @10MHz
IIP3	-22	-16	-19

The final SOC DUT phase noise performance is determined by what type of modulation is imposed on the signal and the information the signal is required to carry. Higher data rates and wider bandwidths of standards, such as 802.11a/g and WCDMA, result in more complex modulation formats, which require increasingly stringent phase noise specifications through out the oscillator chain. Table 1 shows critical system parameters for various standards for today's wireless applications. Note that for increasing modulation complexity (left to right within table) the phase noise specification becomes more stringent.

Figure 3 shows three error vector magnitude (EVM) constellations for a 16-QAM digitally modulated signal as used in a WLAN 802.11a/g application. Specifically it shows that EVM accuracy improves as the phase noise of the LO signal (derived from the reference clock/PLL circuitry) gets better. When the phase noise spectrum in the frequency domain is infinitely narrow, the ideal constellation, with no noise and perfect symmetry, in Figure 3a results. In figures 3b and 3c, the EVM constellation is shown where the phase noise of the LO was deliberately impaired to –64 dBc/Hz and –87 dBc/Hz, respectively. In the worst case, Figure 3b there is so much noise that it is nearly impossible to determine the proper location of the individual constellation points.

The case of Figure 3c has a key point to make. Once the phase noise gets below a certain value, any further improvement in device performance is modest (EVM resulting from this constellation is 1.5% and is better than the EVM specifications for OFDM systems). Increasing the number of samples of the symbols for averaging improves measurements further at the expense of time. Improving the phase noise beyond this point often only reduces the margins for the EVM test. Failing production tests at this point from phase noise effects would more likely be from other phase-sensitive parameters such as adjacent channel selectivity, blocker testing, and noise power ratio.

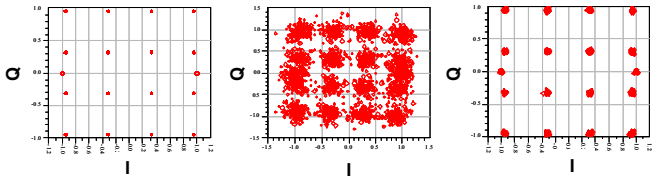

Figure 3 Impact of degraded phase noise on EVM of a digitally modulated signal.

Differences Between CW Sinusoid and "Digital" Sinusoid

Traditionally, the signal used as an analog reference has been a cw sine wave, easily obtained from a crystal oscillator or signal generator. For the particular case of a reference signal, such as that used for a PLL circuit, it is the stable edge transition that is needed, therefore the digital signal is quite well-suited for the application. Figure 4 shows differences between edge transitions (time domain) in a pure sine wave and in a digital waveform, such as that created from a digital pin of an SOC tester.

Because the digital waveform is a square wave (50% duty cycle, in this case), it has more frequency components than the pure sine wave. In some instances, it may be necessary to provide a filter or filter circuit on the load board to reduce the frequency content.

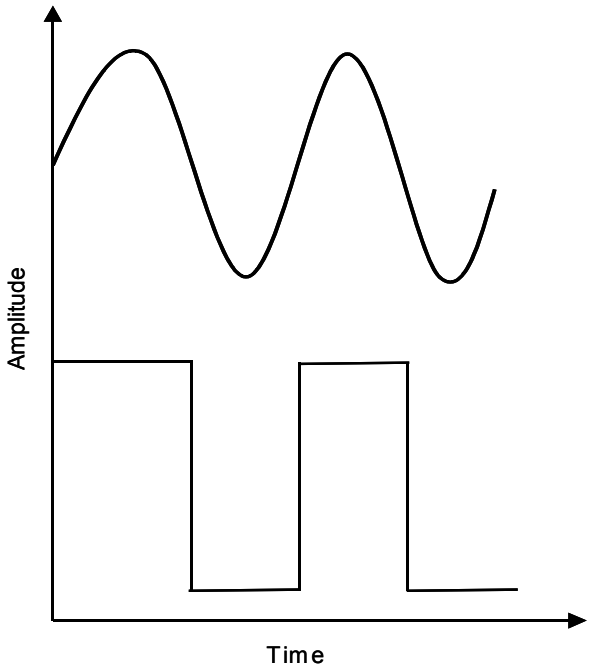

Figure 4 Edge transition differences between analog and digitally generated sinusoidal waveforms.

SOC Test System Architectures

There are many SOC test systems on the market today and all contain some combination of digital, analog, and RF resources. SOC test systems have many more digital pins than analog and RF resources. In many cases, the test system can easily produce most digital patterns required for the wireless radio chipsets. There are many advantages to using a digital system in that there is synchronization with all digital and analog circuitry composing the radio. Additionally, there is increased flexibility to examine chip performance over a wider range of clock signals and the test time is reduced since there is no longer a requirement to capture and evaluate digital results from asynchronous sources.

Data and Results

In a fully configured test system, there are two primary options to provide a reference clock signal to a DUT; an analog signal generator and a digital pin. Using a digital pin of an SOC test system and the signal generator in that same test system, a CDMA signal was generated for a receiver application requiring a reference clock at 19.2 MHz. Table 2 compares the results. As can be seen the results are comparable and either source would be sufficient.

Table 2: Phase noise for a digital pin and a signal generator in an SOC test system

Offset	Digital Pin	Signal Generator
1 kHz	-83 dBc/Hz	-82 dBc/Hz
10 kHz	-105 dBc/Hz	-101 dBc/Hz

In the end, due to resource availability, the digital pin was used to generate the reference clock signal for the phase locked loop control of an RF to baseband cellular receiver, leaving the signal generator available for other uses.

In Figure 5, the phase noise plot of the digital pin shows some interesting characteristics. Without spurious signals included in the plot, the phase noise shown is essentially flat from 1 kHz to 50 kHz. This is a result of the SOC tester's phase lock loop filtering action suppressing the phase noise. From 100 kHz on out, the phase noise is typically less than –120 dBc/Hz.

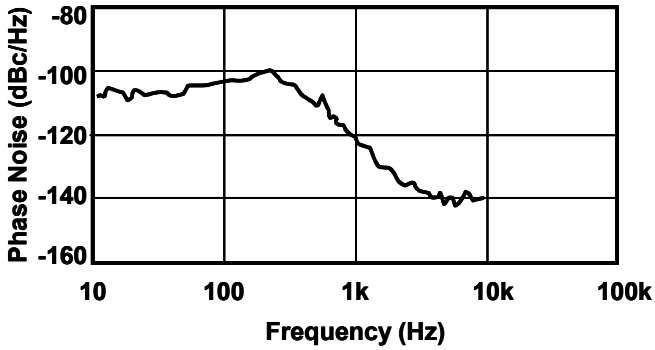

Figure 5 Plot of phase noise of a digital pin from an SOC test system.

To improve the phase noise performance even further, a frequency divider circuit may be implemented on the load board. This would allow the phase noise to be reduced by the relation,

$$\Delta_{\text{phase noise}} = 20\log_{10}(N) \qquad (1)$$

where N is the ratio of the output frequency to the reference frequency (e.g. PLL 'scaling up' a reference). It is important to point out that physical factors limit the actual improvement. Careless use of amplifiers in the divider circuitry and certain types of dividers may actually hamper any gains at all.

From Equation (1) the general rule that for every doubling of frequency, phase noise is increased by 6 dB can be found. More pertinent to this discussion however, the converse also holds, that for every halving of frequency, phase noise is reduced by 6 dB. As an example, if one needs a signal at 20 MHz, there are multiple ways to acquire that. One way is to run the clock at 20 MHz. An alternative, using a frequency divider circuit on the load board, is to run the clock at 80 MHz, using a "divide by 4" circuit, thereby acquiring 12 dB better phase noise performance than that of the 80 MHz signal, due to the frequency division.

As an illustration, Figure 6 shows two different phase noise traces. One is that of a 400 MHz digital signal (50% duty cycle). The second shows the phase noise of that signal after having been divided down to 40 MHz. Note the divided circuit trace has about 18 dB better phase noise across the spectrum, closely reflecting Equation (1).

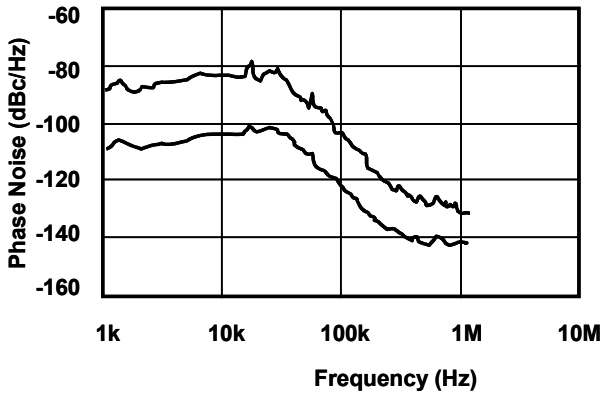

Figure 6 Phase noise offset frequency plots showing the effects of a frequency divider.

Conclusions

A well-characterized waveform in the frequency domain can be used for many signals in device testing. The importance of knowing and understanding the frequency domain characteristics enables the test engineer to determine the usefulness and applicability of the signals for the application.

References

1. Barrett, C., "Fractional/Integer-N PLL Basics," Texas Instruments technical brief SWRA029 (1999).
2. Ferre-Pikal, E. et al., "Draft Revision of IEEE STD 1139-1988 Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology – Random Instabilities," Proceedings of 1997 IEEE International Frequency Control Symposium, pp. 338-357 (1997).